

## Oscillator terms and application notes

### TRI-STATE CONTROL IN CRYSTAL OSSCILLATORS

Most digital systems use the binary number system represented by two state levels 0 and 1. In some special applications, a third-state (Hi Impedance output) is required. A three-state output, or tri-state enable / disable function is available in TTL, HCMOS, or HCMOS crystal oscillators. Its common applications include automated testing, bus wiring data transfer.

The three states are low, high, and high impedance (Hi Z or floating). An output in the hi-impedance state behaves as if it is disconnected from the circuit except for possibly a small leakage current. Three-state devices have an enable / disable input, usually on pin 1 of almost any package. When enable is high or left floating, the device oscillates (with high and low outputs), and when pin 1 is grounded (logic "0"), the device goes into its high-impedance state.

A bus is a common set of wires, usually used for data transfer. A three-state bus has several three-state outputs wired together. With control circuitry, all devices on the bus except one have outputs in the high impedance state. The remaining device is enabled, driving the bus with high and low outputs.

Other applications for a tri-state function is for Automated Testing Equipment (ATE). Outputs of several oscillators are wired together. With control circuitry, all oscillators but one have outputs in the high impedance state. The only oscillator which is selected will have its frequency read out from the counter. (Fig. 5)

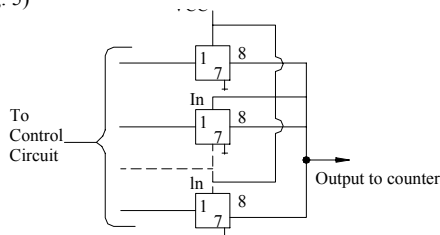


Figure 5

There is always some delay before the tri-state function goes into effect. This effect occurs on both transitions (at disable and at enable). The output disable time of a tri-state from LOW level is  $t_{pLZ}$  and the output enable time of a tri-state to LOW level is  $t_{pZL}$ . (Fig. 6)

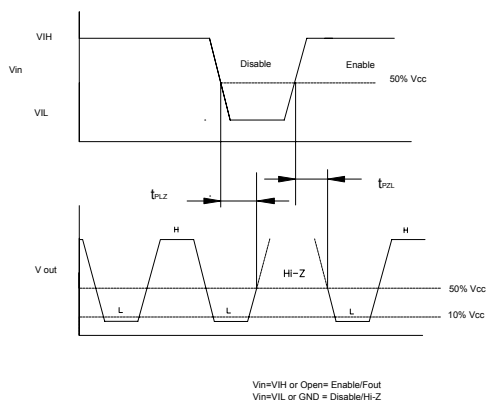


Figure 6

### CMOS RISE AND FALL TIMES

The rise and fall time on the CMOS technology depends on its speed (CMOS, HCMOS, ACMOS, BICMOS), the supply voltage, the load capacitance, and the load configuration. Typical rise and fall time for CMOS 40000 series is 30ns, HCMOS is 6ns, and for ACMOS (HCMOS, TTL compatible) is 3 ns max. Typical rise and fall time is measured between 10% to 90% of its waveform level. (See Fig. 7)

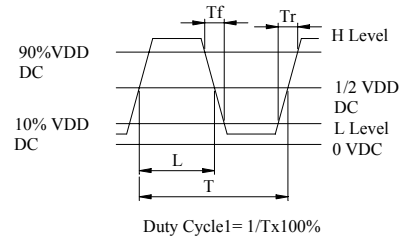


Figure 7

### ACMOS OUTPUT TERMINATION TECHNIQUES

Due to the fast transition time of the ACMOS (HCMOS/TTL compatible) device, proper termination techniques must be used when testing or measuring electrical performance characteristics. Termination is usually used to solve the problem of voltage reflection, which essentially causes steps in clock waveforms as well as overshoot and undershoot. This could result in false clocking of data, as well as higher EMI and system noise.

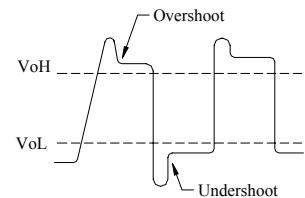


Figure 8

Termination is required also because of the length of the trace on the PC board and its load configuration. There are three general methods of terminating a clock trace, which is a process of matching the output impedance of the device with the line impedance:

**Method 1:** Series termination (Fig. 9) In series termination, a damping resistor is placed close to the source of the clock signal. Value of  $R_s$  must satisfy the following requirement:  $R_s \geq Z_T - R_o$

**Method 2:** Pull-up/Pull-down resistors (Fig. 10) In pull-up/pull-down termination, the Thevenin equivalent of the combination is equal to the characteristics impedance of the trace. This is probably the cleanest, and results in no reflections, as well as reduced EMI.  $R_T \sim Z_T$